AMENDMENTS TO THE CLAIMS

Claims 1-20 (Previously Cancelled).

21. **(CURRENTLY AMENDED)** A method of fabricating a semiconductor device having a semiconductor region, the method comprising the steps of:

forming at least two conductive posts overlying the semiconductor region by at least a lift-off step to form a structure;

encapsulating the structure and at least one of the at least two conductive posts to form a planarized cured passivation layer; and

exposing the at least one of the at least two conductive posts protrudingly through the planarized cured passivation layer to form the semiconductor device[, wherein the step of forming at least two conductive posts comprises a lift-off step].

22. **(PREVIOUSLY AMENDED)** The method of Claim **21**, wherein at least one of the at least two conductive posts comprise at least one of Pt, Au and Ti.

23. **(PREVIOUSLY AMENDED)** The method of Claim **21**, wherein the step of encapsulating the structure and at least one of the at least two conductive posts comprises the steps of:

forming the passivation layer by spinning on benzocyclobutene ("BCB"); and

heating the passivation layer in an N_2 atmosphere to a temperature substantially in the range of 250-350°C for a period substantially in the range of 1-30 minutes, the passivation layer spun on, cured and planarized.

24. **(ORIGINAL)** The method of Claim **21**, wherein the step of exposing the at least one of the at least two conductive posts comprises the step of etching the planarized cured passivation layer.

25. **(PREVIOUSLY AMENDED)** The method of Claim **32**, wherein the Reactive Ion Etching step employs a chemistry of at least one of CF_4:O_2 at an approximate ratio of 40:60 and SF_6:O_2 at an approximate ratio of 6:10.

26. **(CURRENTLY AMENDED)** A method of fabricating a semiconductor device having a semiconductor region, the method comprising the steps of:

forming at least two conductive posts of about the same height <u>by at least a lift-off step</u> overlying the semiconductor region to form a structure;

encapsulating the structure and [at least one of] the at least two conductive posts to form a planarized cured passivation layer; and

exposing the [at least one of] the at least two conductive posts <u>protrudingly</u> through the planarized cured passivation layer to form the semiconductor device[, wherein the step of forming at least two conductive posts comprises a lift-off step].

27. **(PREVIOUSLY AMENDED)** The method of Claim **26**, wherein at least one of the at least two conductive posts comprises at least one of Pt, Au and Ti.

28. **(PREVIOUSLY AMENDED)** The method of Claim **26**, wherein the step of encapsulating the structure and at least one of the at least two conductive posts comprises the steps of:

forming the passivation layer by spinning on benzocyclobutene ("BCB"); and

heating the passivation layer in an N_2 atmosphere to a temperature substantially in the range of 250-350°C for a period substantially in the range of 1-30 minutes, the passivation layer spun on, cured and planarized.

29. **(ORIGINAL)** The method of Claim **26**, wherein the step of exposing the at least one of the at least two conductive posts comprises the step of etching the planarized cured passivation layer.

30. **(PREVIOUSLY AMENDED)** The method of Claim **29**, wherein the step of etching the planarized cured passivation layer comprises a Reactive Ion Etching step.

31. **(PREVIOUSLY AMENDED)** The method of Claim **30**, wherein the Reactive Ion Etching step employs a chemistry of at least one of CF_4:O_2 at an approximate ratio of 40:60 and SF_6:O_2 at an approximate ratio of 6:10.

32. **(PREVIOUSLY ENTERED)** The method of Claim **24**, wherein the step of etching the planarized cured passivation layer comprises a Reactive Ion Etching step.

33. **(NEW)** The method of Claim **21**, wherein the step of exposing reduces a height of the planarized cured passivation layer beneath or equal to a height of the at least one of the at least two conductive posts.

34. **(NEW)** The method of Claim **26**, wherein the step of exposing reduces a height of the planarized cured passivation layer beneath or equal to a height of the at least one of the at least two conductive posts.

35. **(NEW)** A method of fabricating a semiconductor device having a semiconductor region, the method comprising the steps of:

forming at least one conductive post overlying the semiconductor region to form a structure;

encapsulating the structure and the at least one conductive post to form a planarized cured passivation layer; and

etching the planarized cured passivation layer causing the encapsulated at least one conductive post to protrude through the planarized cured passivation layer and form the semiconductor device.

36. **(NEW)** The method of Claim **35**, wherein the step of etching reduces a height of the planarized cured passivation layer beneath or equal to a height of the at least one conductive post.

37. **(NEW)** The method of Claim **36**, wherein the step of etching comprises:

masking a portion of the encapsulated structure, the portion corresponding with a position of the encapsulated at least one conductive post.